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Proceedings of the 2018 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 129-132

eISBN: 978-1-5386-7392-8

ISSN: 1558-3899

DOI: <https://doi.org/10.1109/MWSCAS.2018.8624059>

Accepted manuscript

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All-Pass Time Delay Circuit Magnitude Response Optimization Using Fractional-Order Capacitor

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Abstract—Paper presents the integer- and fractional-order cases of a voltage-mode all-pass time delay circuit, or more frequently called as all-pass filter, employing a single negative-type current-controlled current inverting transconductance amplifier and a floating capacitor. Utilization of a fractional-order capacitor (FoC) $C_{0.96}$ with $12 \text{ pF} \cdot \text{sec}^{-0.04}$ value for magnitude response optimization of the filter is investigated. FoC was emulated via 4th-order Valsa RC network and values optimized using modified least squares quadratic method. In frequency range 1 MHz–1 GHz it shows only ± 0.5 degree phase angle deviation and the relative pseudo-capacitance error varies from -1.85% to $+0.73\%$. SPICE simulations are given to prove the theory.

Keywords—all-pass filter; CCCITA–; fractional-order capacitor; FoC; fractional-order filter; time delay circuit; voltage-mode

I. INTRODUCTION

First-order all-pass time delay circuit or so-called all-pass filter (APF) is widely used in analog signal processing in order to shift the phase of an electrical signal while keeping the amplitude constant [1]–[5]. Such circuits have several useful applications, for instance, broadband beamformers, equalizing the communication channel for wire-line communication, oscillator design, etc. [3]–[5]. Ideally, APFs should have both a constant unity gain and a well-defined constant delay. Although in practice circuits employing only grounded capacitors are preferred, new IC technologies offer floating capacitor realization easy way as a double poly or metal-insulator-metal capacitor [6]. Another issue regarding capacitors is their order. As it was shown [7], readily available capacitors do not behave as pure components. For an instance, experimentally measured order of capacitor based on polyvinylidene fluoride is 0.9776, metalized paper of 0.9821, etc. Currently, these so-called fractional-order capacitors (FoCs) are one of the most crucial elements used for electronic circuit and systems design and there is a growing research interest in development of these components [8]–[11] (and references cited therein). Therefore, this paper aims to introduce a utilization of FoC for magnitude response optimization of the proposed first-order

APF. Introduced theory and the workability of 0.96 and first-order resistorless filter were verified by SPICE simulations.

II. CIRCUIT DESCRIPTION

A. Negative-Type Current-Controlled Current Inverting Transconductance Amplifier (CCCITA–)

The CCCITA–, which circuit symbol is depicted in Fig. 1(a), is a three-terminal device [12]. It consists of an input negative current-controlled current inverter stage that transfers the input current to the z terminal and an operational transconductance amplifier stage, which converts the voltage at the z terminal to output current at the x – terminal. Using a standard notation, it can be described by the following set of equations:

$$v_f = R_f i_f, \quad i_z = -i_f, \quad i_{x-} = -g_m v_z, \quad (1)$$

where R_f and g_m represent the intrinsic resistance of f terminal and transconductance gain from the z terminal to x – terminal, respectively.

Taking into account parasitics of CCCITA– depicted in Fig. 1(b), the following non-idealities of the active element must be considered:

- Parasitic resistances R_z , R_{x-} and capacitance C_z , C_{x-} appearing between the high-impedance z and x – terminals and ground, respectively,
- $i_z = -\beta i_f$, where β represents current gain that differs from its ideally unity value by current tracking error ε_i ($|\varepsilon_i| \ll 1$).

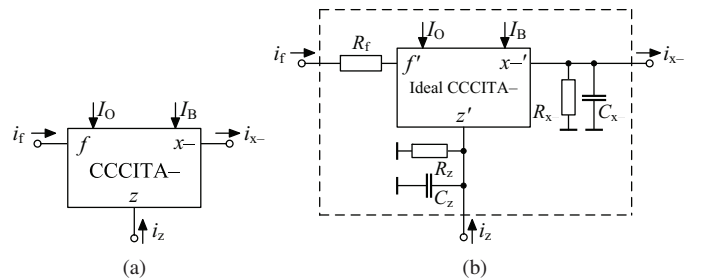


Fig. 1. CCCITA–: (a) circuit symbol, (b) its main parasitic components.

This article is based upon work from COST Action CA15225, a network supported by COST (European Cooperation in Science and Technology). Research described in this paper was financed by the National Sustainability Program under grant no. LO1401 and by the Czech Science Foundation under grant no. 16-11460Y. For the research, infrastructure of the SIX Center was used.

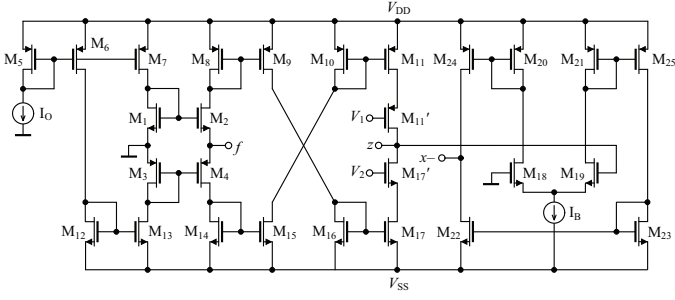


Fig. 2. CMOS internal structure of CCCITA-.

In CMOS implementation of CCCITA- shown in Fig. 2, the intrinsic resistance and the transconductance are respectively given as $R_f = \sqrt{1/(8k_1 I_O)}$ and $g_m = \sqrt{k_2 I_B}$, where $k_1 = \mu_p C_{ox} (W/L)_{3,4} = \mu_n C_{ox} (W/L)_{1,2}$ and $k_2 = \mu_n C_{ox} (W/L)_{18,19}$. Here the $k_i = \mu_{p,n} C_{ox} (W/L)_j$ for $i = 1, 2$ is the physical parameter of the corresponding MOS transistor j (C_{ox} is the gate oxide capacitance per unit area, $\mu_{p,n}$ is the electron mobility in the channel, W and L are the channel width and length), the I_O is the bias current to control the intrinsic resistance of the input terminal f , and the I_B is the control current adjusting the transconductance g_m of the CCCITA-.

B. First-(Integer)-Order All-Pass Filter Design

The proposed realizations of a resistorless VM APF using single CCCITA- and a one floating capacitor is shown in Fig. 3. Using (1), routine circuit analysis yields a voltage transfer function (TF) in the following form:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{sC - g_m}{sC + \frac{1}{R_f}}, \quad (2)$$

which indicates a TF of first-order APF with an inverting response. Considering the fact that there is a capacitor connected between the filter's input and output terminals and the capacitor behaves as a short-circuit element at the very high frequencies, the filter features with very accurate unity magnitude in this frequency region. On the other hand, at very low frequencies, the filter magnitude approximates to $V_{out}/V_{in}|_{s=0} = -g_m R_f$.

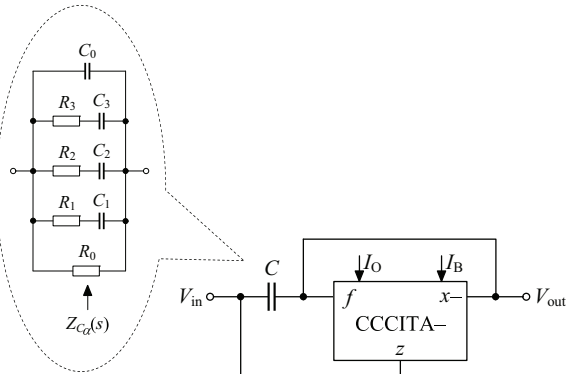


Fig. 3. Proposed voltage-mode all-pass filter.

Hence, assuming parameter matching $g_m = 1/R_f$ the gain is again unity. Note that the same interesting and useful property can be found in filters [2] and [4].

Now, from (2) the phase response of the filter is given as:

$$\varphi(\omega) = \arctan \left[\frac{\omega C (g_m R_f + 1)}{\omega^2 C^2 R_f - g_m} \right], \quad (3)$$

hence, the phase of voltage TF alters from 180° to 0° while ω changes from $0 \rightarrow \infty$. Finally, the resulting ideal pole (ω_p) and zero (ω_z) frequencies can be expressed as:

$$\omega_p = \frac{1}{C R_f}, \quad \omega_z = \frac{g_m}{C}. \quad (4)$$

From (4) it is evident that the ω_p and ω_z sensitivity to passive elements and active parameter are unity in relative magnitude as $S_C^{\omega_p, \omega_z} = S_{R_f}^{\omega_p} = -1$, $S_{g_m}^{\omega_z} = 1$.

For a complete analysis, it is important to take into account parasitic resistances and capacitance of the active element given in Fig. 1(b). Hence, the ideal TF in (2) converts to:

$$T'(s) = \frac{V_{out}}{V_{in}} = \frac{sC - g_m}{sC' + \frac{1}{R'}}, \quad (5)$$

and non-ideal phase response from TF (5) is given as:

$$\varphi'(\omega) = \arctan \left\{ \frac{\omega [R_{x-} (C + g_m R_f C') + C R_f]}{R_{x-} (R_f \omega^2 C C' - g_m) - g_m R_f} \right\}. \quad (6)$$

Consequently, the pole frequency of the filter is found as:

$$\omega'_p = \frac{1}{C' R'}, \quad (7)$$

while ω_z remains as (4) and in (5)–(7) the $C' = C + C_{x-}$ and $R' = R_f \parallel R_{x-}$. Note that the filter still has a very accurate unity magnitude at very low and very high frequencies, because typical value of R_{x-} is much larger than $1/g_m$ or R_f . On the other hand, as it will be shown in Section III, possible mismatch between ω'_p and ω_z can be compensated with a FoC.

C. All-Pass Filter Utilization Using FoC

Considering the proposed VM APF given in Fig. 3 employing a non-ideal CCCITA- and assuming replacement of integer-order capacitor C by a fractional-order (FO) one with pseudo-capacitance C_α ($0 < \alpha < 1$) of impedance $Z_{C_\alpha}(s) = 1/C_\alpha s^\alpha$, the TF in (5) turns to:

$$T'_\alpha(s) = \frac{V_{out}}{V_{in}} = \frac{s^\alpha C_\alpha - g_m}{s^\alpha C_\alpha + \frac{1}{R_f} + Y_{x-}}. \quad (8)$$

Now, to evaluate the phase response, $\omega'_{p,\alpha}$, and $\omega'_{z,\alpha}$, the s^α is replaced by $\omega^\alpha [\cos(\alpha\pi/2) + j \sin(\alpha\pi/2)]$. Therefore, the resulted expressions in (9)–(11) are:

$$\omega'_{p,\alpha} = \left\{ \frac{(1 + R_f Y_{x-}) \left[-\cos\left(\frac{\alpha\pi}{2}\right) - \sqrt{\cos^2\left(\frac{\alpha\pi}{2}\right) - 1} \right]}{R_f C_\alpha} \right\}^{1/\alpha}, \quad (10)$$

$$\varphi'_\alpha(\omega) = -\arctan \left\{ \frac{[R_f(g_m + Y_{x-}) + 1] \sin\left(\frac{\alpha\pi}{2}\right) C_\alpha \omega^\alpha}{[R_f(g_m - Y_{x-}) - 1] \omega^\alpha C_\alpha \cos\left(\frac{\alpha\pi}{2}\right) + g_m R_f Y_{x-} - \omega^{2\alpha} C_\alpha^2 R_f + g_m} \right\}, \quad (9)$$

$$\omega'_{z,\alpha} = \left\{ \frac{g_m \left[\cos\left(\frac{\alpha\pi}{2}\right) - \sqrt{\cos^2\left(\frac{\alpha\pi}{2}\right) - 1} \right]}{C_\alpha} \right\}^{1/\alpha}. \quad (11)$$

Here it is important noting that the parasitic admittance Y_{x-} appearing at $x-$ terminal has an integer-order character. Therefore, it must be assumed as $sC_{x-} + 1/R_{x-}$ due to difference in capacitances of C_α and C_{x-} from their nature (see [11]).

III. SIMULATION RESULTS

To verify the theoretical study, the proposed resistorless VM APF in Fig. 3 has been simulated using SPICE software. The CMOS implementation of the CCCITA- shown in Fig. 2 was modified from [12]. In the design, transistors are modeled by the TSMC 0.35 μm level-3 CMOS process parameters [12]. Dimensions of transistors are listed in Table I. The DC power supply voltages are equal to $+V_{DD} = -V_{SS} = 1.5$ V and $V_1 = V_2 = 0$ V. The intrinsic resistance at input terminal R_f and transconductance gain g_m value were set as $I_O = 12.4$ μA and $I_B = 36$ μA , respectively, in order to fulfill the above discussed parameter matching $g_m = 1/R_f \cong 1$ mA/V.

First of all, the workability of the proposed integer-order VM APF was verified. Capacitor value was selected as $C = 5.7$ pF, which resulted in a 90° phase shift at pole frequency $f_{p,id} = 27.9$ MHz. Figure 4(a) shows the ideal and simulated gain and phase responses of the proposed filter. Note that the obtained $f_{p,sim}$ is equal to 27.3 MHz, which is close to calculated one. Time-domain simulation result is shown in Fig. 4(b). In simulations, a sine-wave input of 150 mV amplitude and frequency of $f_{p,sim}$ was applied to the filter.

TABLE I. TRANSISTOR DIMENSIONS OF CCCITA- IN FIG. 2.

PMOS transistors	W(μm)/L(μm)
M ₃ , M ₄	60/0.35
M ₅ -M ₇	30/2
M ₈ -M ₁₁ , M ₁₁	30/1
M ₂₀ , M ₂₁	2/0.5
M ₂₄ , M ₂₅	8/0.5
NMOS transistors	W(μm)/L(μm)
M ₁ , M ₂	20/0.35
M ₁₂ -M ₁₇ , M ₁₇	10/1
M ₁₈ , M ₁₉	5/0.5
M ₂₂ , M ₂₃	2/0.5

TABLE II. PARAMETERS OF THE $C_{0.96}$ EMULATOR DEPICTED IN FIG. 3. (NOTE: # IN 1 MHz-1 GHz RANGE)

Component values (k Ω) / (pF)							
R_0	R_1	R_2	R_3	C_0	C_1	C_2	C_3
511	46.4	0.562	5.62	4.7	0.6	0.5	0.5
Total resistance (k Ω) / capacitance (pF)							
563.6				6.3			
Spread of resistance / capacitance							
909.3				9.4			
Order α (–) / phase (degree) / C_α (pF·sec $^{\alpha-1}$)							
0.96 / – 86.4 / 12							
Theoretical phase angle deviation [#] (degree) / relative C_α error [#] (%)							
± 0.5 / – 1.85 \rightarrow +0.73							

The total harmonic distortion (THD) is found as 2.65%. As it can be from the results observed, due to mismatch between ω'_p and ω_z , a deviation in gain of integer-order APF occurred. The obtained discrepancy in gain of the APF was compensated with a FoC. MAPLE plot given in Fig. 5(a) shows the effect of FoC order in range $\alpha = \{0.75 \text{ to } 1\}$ on magnitude of the FO filter. As it can be observed, a FoC of an order 0.96 should be used to suppress the deviation in gain of the integer-order APF. Subsequently, the effect of parameter matching $g_m = 1/R_f$ on magnitude of 0.96-order filter is shown in Fig. 5(b) while R_f was kept 1 k Ω . Hence, small change in values causes significant discrepancy. Optimized Valsa RC network realization was used to realize $C_{0.96}$, which is depicted in Fig. 3. It provides a 4th-order approximation of FoC, which has an admittance in the following general form:

$$Y_{C_\alpha}(s) = 1/Z_{C_\alpha}(s) = 1/R_0 + \sum_{k=1}^3 sC_k/[sR_kC_k + 1] + sC_0.$$

Component values obtained via modified least squares quadratic (MLSQ) method and parameters of $C_{0.96}$ emulator are listed in Table II. Theoretical and simulated phase and pseudo-capacitance versus frequency are given in Fig. 6 and their ideal values are $\varphi_{0.96} = -86.4$ degree and $C_{0.96} = 12$ pF $\cdot\text{sec}^{-0.04}$, respectively. The equivalent equations for fitting the phase or pseudo-capacitance via linear regression are provided inside Figures. As it can be seen, in frequency range 1 MHz-1 GHz it shows only ± 0.5 degree phase angle deviation and corresponding relative pseudo-capacitance error varies from -1.85% to +0.73%. Simulated phase and gain responses vs. frequency and time-domain responses of the APF are compared with integer-order one in Fig. 4(a) and (b),

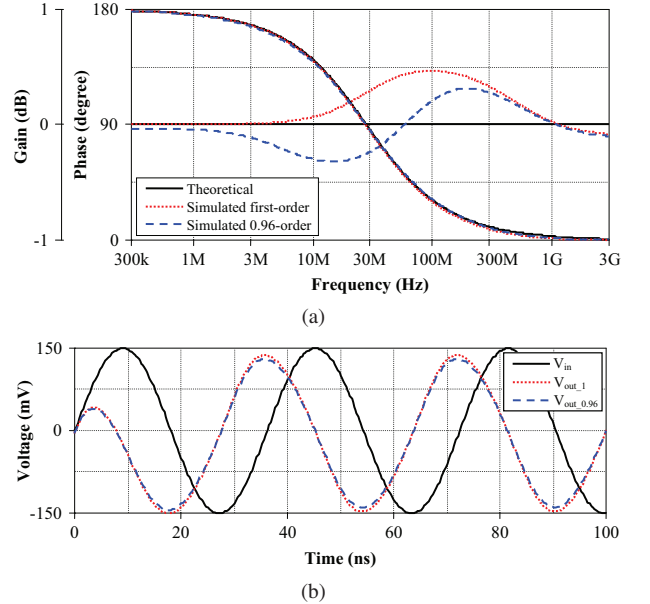


Fig. 4. Theoretical (ideal) and simulated (a) gain and phase responses, (b) time-domain responses of proposed VM APF of orders $\alpha = [0.96; 1]$.

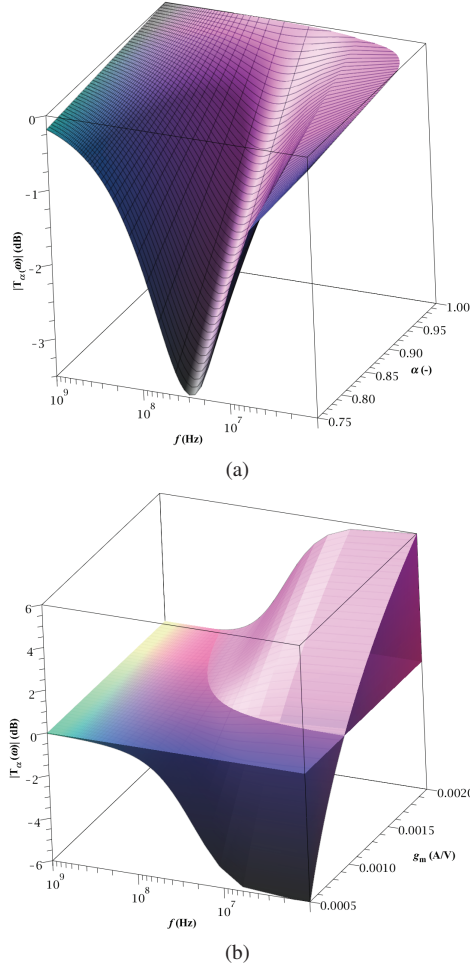


Fig. 5. Effect on magnitude of the VM APF: (a) α vs. frequency, (b) g_m vs. frequency at $C_{0.96}$.

respectively. As it can be observed, the deviation in gain of integer-order APF was compensated, while the phase shift at $f_{p_sim,\alpha}$ remained close to 90° . Obtained $THD_{0.96}$ value of the output waveform yields 2.62%. Finally, the comparison of relative gain error of first- and 0.96-order APFs is given in Fig. 7. Based on the simulation results it can be stated that the error at $f_{p_sim,\alpha}$ is lower for 0.96-order APF.

IV. CONCLUSION

The paper presented a magnitude response optimization of a VM APF using a FoC. The $C_{0.96}$ with $12 \text{ pF} \cdot \text{sec}^{-0.04}$ value was emulated via 4th-order Valsa RC network, which after optimization using MLSQ method, indicates broadband constant phase and pseudo-capacitance performance. The theory and the behavior of APF were verified using SPICE simulations.

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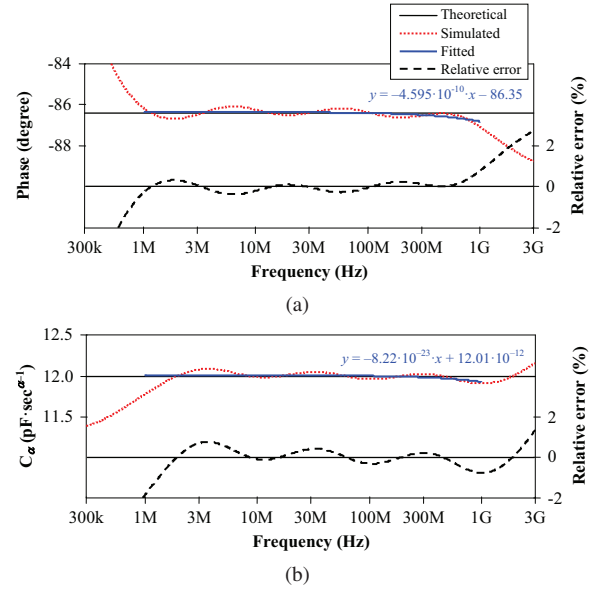


Fig. 6. 0.96-order FoC: (a) Phase, (b) pseudo-capacitance, and relative errors vs. frequency.

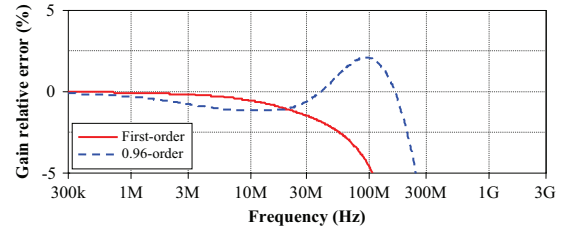


Fig. 7. Relative error in gain of first- and 0.96-order VM APFs.

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